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10/647,223	08/26/2003	Takashi Miyazawa	116921	1896

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EXAMINER	
SHERMAN, STEPHEN G	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 05/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/647,223	MIYAZAWA, TAKASHI	
	Examiner	Art Unit	
	Stephen G. Sherman	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28 and 32-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *36* is/are allowed.

6)☒ Claim(s) *1,2,5-16,19,20,22,24-28,32-35 and 37-39* is/are rejected.

7)☒ Claim(s) *3,4,17-18,21 and 23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment filed the 16 February 2006. Claims 1-28 and 32-39 are pending. Claims 29-31 have been cancelled.

Response to Arguments

2. Applicant's arguments with respect to claims 15, 36 and 37 have been considered but are moot in view of the new ground(s) of rejection.

3. Applicant's arguments with respect to claims 1, 11 and 19 filed 16 February 2006 have been fully considered but they are not persuasive. The applicant argues Akimoto fails to teach "wherein an electrically conductive state of the first transistor being set during at least part of a first period in which the data line is electrically connected to the second electrode through the third transistor." The examiner respectfully disagrees.

As recited in the previous office action, Figure 10 of Akimoto shows a third transistor 71 that has one terminal connected to the data line 77 and its gate connected to the gate line 83. Figure 10 also shows a first transistor 74, which has a gate electrode connected to the first electrode of capacitor 72. As paragraph [0087] of Akimoto states, during the "write period" third transistor 71 is "turned on" meaning that the signal from the data line 77 is applied to the second electrode of capacitor 72. During this same "write period" the voltage line 18 puts the first transistor 74 into the

conductive state, meaning that during the same period of time the conductive states of the first transistor is set during at least part of a first period in which the data line is electrically connected to the second electrode through the third transistor.

Claim Objections

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 15 recites the limitation "the data signal." There is insufficient antecedent basis for this limitation in the claim.

6. Claim 16 recites the limitation "the driving transistor." There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1-2, 5-14, 19, 22, 24-25, 32-35 and 37-39 are rejected under 35 U.S.C. 102(e) as being anticipated by Akimoto et al. (US 2003/0067424).

Regarding claim 1, Akimoto et al. disclose an electronic circuit (Figure 10) comprising:

a plurality of unit circuits (Figure 10, unit circuits 70);

a first power source line (Figure 10, line 79 is a power source line since as stated in paragraph [0083] it receives both the scanning output and a light on control line, which would both contain a voltage since a voltage would need to be applied to the gate of control transistor 76 in order to turn the transistor on.); and

a control circuit that sets a potential of the first power source line to a plurality of potentials or controls an electrical disconnection and an electrical connection between the first power source line and a predetermined voltage (Figure 10, items 76 and 80 make up a control circuit, where item 80 sets the potential of the power source line 79.),

each of the plurality of unit circuits including:

a first transistor having a first terminal, a second terminal, and a first control terminal (Figure 10, transistor 74);

a second transistor having a third terminal, a fourth terminal, and a second control terminal (Figure 10, transistor 75), the third terminal and the fourth terminal being coupled to the first control terminal and the first power source line, respectively (Figure 10 shows that one terminal of transistor 75 is coupled to the gate of transistor 74 and that the other terminal of transistor 75 is coupled to the power source line 79 through the control transistor 76.);

a capacitive element having a first electrode and a second electrode (Figure 10, capacitor 72), the first electrode being coupled to the first control terminal (As shown in Figure 10, capacitor 72 has a first electrode coupled to the control terminal of transistor 74.); and

a third transistor having a fifth terminal and a sixth terminal (Figure 10, transistor 71), the third transistor controlling an electrical connection between a data line and the second electrode (As paragraph [0087] of Akimoto states, during the "write period" third transistor 71 is "turned on" meaning that the signal from the data line 77 is applied to the second electrode of capacitor 72.), and

an electrically conductive state of the first transistor being set during at least a part of a first period in which the data line is electrically connected to the second electrode through the third transistor (As stated above, paragraph [0087] of Akimoto states, during the "write period" third transistor 71 is "turned on," meaning that the signal from the data line 77 is applied to the second electrode of capacitor 72. During this same "write period" the voltage line 18 puts the first transistor 74 into the conductive state, meaning that during the same period of time the conductive states of the first

transistor is set during at least part of a first period in which the data line is electrically connected to the second electrode through the third transistor.).

Regarding claims 2, 12 and 20, Akimoto et al. disclose the electronic circuit according to claims 1, 11 and 19, further comprising a second power source line that is coupled to the second terminal (Figure 10 shows that power source line 18 is coupled to the second terminal of transistor 74.).

Regarding claims 5, 13 and 24, Akimoto et al. disclose the electronic circuit according to claims 1, 11 and 19.

Akimoto et al. also disclose of the conductive types of the first transistor and the second transistor being equal to each other (Figure 10.The examiner interprets that the transistors shown in the figure are of the same type since on page 6, paragraph [0083] it is stated that item 74 is a p-channel MOS transistor and transistors 74 and 75 are drawn the same way in Figure 10.).

Regarding claims 6 and 14, Akimoto et al. disclose the electronic circuit according to claim 1 and 11.

Akimoto et al. also disclose that each of the plurality of unit circuits further including an electronic element coupled to the first terminal (Figure 10, item 7 is coupled to the first terminal of transistor 74 through control transistor 76.).

Regarding claim 7, Akimoto et al. and Matsumoto disclose the electronic circuit according to claim 6.

Akimoto et al. also disclose an electronic element being a current-driven element (Figure 10, OLED 7 is a current driven element.).

Regarding claims 8 and 22, Akimoto et al. disclose the electronic circuit according to claims 1 and 19.

Akimoto et al. also disclose the control circuit being a fourth transistor (Figure 10, transistor 76) having a seventh terminal and an eight terminal (Transistor 76 has two terminals.), the seventh terminal being coupled to the fourth terminal through one first power source line of the plurality of first power source lines, and the eight terminal being coupled to the predetermined voltage (Figure 10 shows that control transistor 76 has a terminal connected to the OLED 7 that is coupled to the terminal of transistor 75 through the power source line 79 connected to the gate of transistor 76. The examiner understands that since the power source line 79 control whether the terminals of transistor 76 and 75 as in connection that the terminals are coupled by the line. The other terminal of transistor 76 is coupled to the predetermined voltage of power source 79 through the gate of the transistor.).

Regarding claim 9, Akimoto et al. disclose the electronic circuit according to claim 2, the second power source line being set a the predetermined voltage (Figure 10, power source line 18 is set to a predetermined voltage as stated in paragraph [0087].

The examiner understands that when Akimoto states "specific voltage" that this means that the voltage is predetermined.).

Regarding claims 10 and 25, Akimoto et al. disclose the electronic circuit according to claims 1 and 19.

Akimoto et al. also disclose of a threshold voltage of the first transistor being set to be not lower than a threshold voltage of the second transistor (Paragraph [0087]. The examiner interprets that since when transistor 75, the second transistor, is turned on the same potential is applied to transistor 74, but that another potential needs to be applied through the power source line to put transistor 74 into a conductive state, that this means that the threshold of transistor 74, the first transistor, is not lower than the second transistor.).

Regarding claim 11, please refer to the rejection of claim 1, and further more Akimoto et al. also disclose:

a plurality of first signal lines (Figure 10, gate lines 83);

a plurality of second signal lines (Figure 10, data lines 77);

a third transistor having a fifth and sixth terminal (Figure 10, transistor 71), and a third control terminal, the third transistor controlling an electrical connection between the second electrode and one second signal line of the plurality of second signal lines (The transistor 71 controls the connection between capacitor 72 and the data line when the transistor is activated as explained in paragraph [0083].), the third control terminal being

coupled to one firth signal line of the plurality of first signal lines (The gate of transistor 71 is connected to the gate line 83.).

Regarding claim 19, please refer to the rejection of claims 11 and 14.

Regarding claim 26, Akimoto et al. disclose the electro-optical device according to claim 20, the one second power source line being coupled to the predetermined voltage (Figure 10, the power source line 18 is coupled to the predetermined voltage on power source line 79 through the terminals of transistor 74 and the terminal and gate of transistor 76.).

Regarding claim 27, Akimoto et al. disclose the electro-optical device according to claim 19.

Akimoto et al. also disclose the electro-optical element being an EL element (Figure 10, item 7. An OLED is an EL element.).

Regarding claim 32, Akimoto et al. disclose the electronic circuit according to claim 1.

Akimoto et al. also discloses of an electronic apparatus being equipped with the electronic circuit according to claim 1 (Page 1, paragraph [0001]).

33. An electronic apparatus being equipped with the electro-optical device according to claim 19.

Regarding claim 33, Akimoto et al. disclose the electro-optical device according to claim 19. Akimoto et al. also discloses of an electronic apparatus being equipped with the electro-optical device according to claim 19 (Page 1, paragraph [0001]).

Regarding claims 34 and 39, Akimoto et al. disclose the electro-optical device according to claims 11 and 19, the plurality of first power source lines intersecting the plurality of data lines (Figure 10 shows that the first power source lines 79 intersect the data lines 77.).

Regarding claim 35, Akimoto et al. disclose the electro-optical device according to claim 19, the plurality of first power source lines being arranged along the plurality of scanning lines (Figure 10 shows that the power source lines 79 are arranged along the gate lines 83.).

Regarding claim 37, this claim is rejected under the same rationale as claim 15.

Regarding claim 38, Akimoto et al. disclose the electronic circuit according to claim 6, a driving voltage and a driving current whose levels correspond to the electrically conductive state of the first transistor are supplied to the electronic element during a second period (Paragraphs [0087]-[0089] explain that a voltage to put the transistor 74 into a conductive state is supplied by voltage line 18, but the gate voltage

of the transistor 74 is then lower to be lower than the voltage to put the transistor into the conductive state. Then the data is written into the pixel circuit an the voltage difference to put the transistor into the conductive state is stored in the capacitor 73. Then is a period later, the voltage is then supplied to the gate on transistor 74 in order to put the transistor back into the conductive state and to end the voltage signals to the OLED 7.).

9. Claims 15-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Dawson et al. (US 6,229,506).

Regarding claim 15, Dawson et al. disclose an electronic circuit comprising:

a first signal line (Figure 2, select line 210);

a second signal line (Figure 2, data line 220);

a power source line (Figure 2, power source line 295 with voltage +VDD.); and

a plurality of unit circuits (Figure 2, item 200 and column 3, lines 4-10 state that although the figures show only one pixel that they could be used in an array.), each of the plurality of unit circuits including:

a first transistor having a first terminal, a second terminal, and a first control terminal (Figure 2, transistor 260 is a first transistor.);

a second transistor having a third terminal that is coupled to the first control terminal and a fourth terminal that is directly connected to the power source line (Figure

2, transistor 270 has a terminal coupled to the gate of transistor 260 through capacitor 280, and has another terminal directly connected to the power source line 295.);

a capacitive element having a first electrode that is coupled to the first control terminal and a second electrode (Figure 2, capacitor 280 is coupled to the gate of transistor 260 through a first electrode and has a second electrode.); and

a third transistor having a fifth terminal that is coupled to the second electrode (Figure 2, a transistor 250 has a terminal that is coupled to the second electrode of capacitor 280.), a sixth terminal that is coupled to the second signal line (The other terminal of transistor 250 is coupled to the data line 220.), and a third control terminal that is coupled to the first signal line (The gate of transistor 250 is coupled to the select line 210.), and

the first electrode being electrically connected to the power source line through the second transistor during a first period before a second period in which the data signal is transmitted to the capacitive element through the third transistor (Column 3, line 30 to column 4, line 24 explains that the circuit operates with two different periods: a load data phase and a continuous illuminating phase, where the load data phase is where the data signal is transmitted to the capacitive element and the illuminating phase is when the capacitor is connected to the power source line. These two periods alternate with each other throughout the driving of the pixel circuit, meaning that after the illuminating phase takes place the load data phase occurs.).

Regarding claim 16, Dawson et al. disclose the electronic circuit according to claim 15. Dawson et al. also disclose an electronic element being connected to the driving transistor (Figure 2, OLED 290 is coupled to the transistor 260.).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

12. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Akimoto et al. (US 2003/0067424) in view of Matsumoto (US 2002/0167504).

Regarding claim 28, Akimoto et al. disclose the electro-optical device according to claim 19.

Akimoto et al. fail to teach of the electro-optical elements of the same color being arranged along the scanning lines

Matsumoto also discloses of the electro-optical elements of the same color being arranged along the scanning lines (Figure 1, R DATA LINE, G DATA LINE and B DATA LINE.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to arrange elements taught by Akimoto et al. into the arrangement as taught Matsumoto such that the elements of the same color would be arranged along the scanning lines in order to create a display which is proper for a miniature portable display such that current consumption is decreased and the layout area of the circuit can also be decreased.

Allowable Subject Matter

13. Claim 36 is allowed.

14. Claims 3-4, 17-18, 21 and 23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

15. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 36, the primary reason for allowance is the inclusion of both the control circuit and the fourth control terminal being directly connected to the first control terminal, with the specific circuit configuration as claimed, which is not found singularly or in combination in the prior art.

Regarding claims 3 and 21, the primary reason for indicating allowable subject matter is the inclusion of the second control terminal being coupled to the third terminal in the specific circuit configuration as claimed, which is not found singularly or in combination in the prior art.

Regarding claims 4, 18 and 23, the primary reason for indicating allowable subject matter is the recitation that there are only three transistors in the unit circuit added to the already claimed circuit configuration, which is not found singularly or in combination in the prior art.

Regarding claim 17, the primary reason for indicating allowable subject matter is the inclusion of the control circuit to the already claimed circuit configuration, which is not found singularly or in combination in the prior art.

Conclusion

16. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen G. Sherman whose telephone number is (571) 272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SS

25 April 2006

AMR A. AWAD
PRIMARY EXAMINER